REMARKS

Dear Sir:

These remarks are in response to the Office Action mailed on May 9, 2003. The Office Action has allowed claims 1-37 and rejected claim 38 under 35 U.S.C. 102(b) as anticipated by Niijima et al. (U.S. patent number 5,457,658). The Applicant thanks the Examiner for allowing claims 1-37 and believes that claim 38 is also allowable for the reasons stated below. The title has been amended along the lines suggested in the Office Action.

With respect to claim 38, it is respectfully submitted that the rejection 35 U.S.C. 102(b) as anticipated by Niijima is not well founded. Claim 38 states:

> A method of operating a non-volatile memory system comprising a controller and a memory, wherein data is stored in the memory based on physical address, the method comprising:
>
> transferring data between a host and the controller based on a logical sector addresses;
>
> *transferring data between the controller and the memory based on the logical sector address;*
>
> *converting on the memory the logical sector address into a corresponding physical sector address*; and
>
> accessing data stored in the memory at the corresponding physical address.

This is believed to differ from Niijima, and the prior art in general, base upon the middle two element which have the added emphasis. As described in the claim, data is exchanged between the controller and memory based on the *logical address*, which is then converted *on the memory* itself into a physical address. This is the reverse of what occurs in the cited prior art, where the logical to physical address conversion takes place *on the controller*, with data then being transferred between the controller and the memory based on the already converter *physical address*. In both cases, the first and last elements of the claim would be the same, but it is the middle two elements that distinguish it from the prior art, resulting in the advantages cited in the application.

More specifically, with respect to Niijima, the Office Action refers to column 2, lines 27-56. The cited portion does refer to a logical to physical address conversion; however, this occurs on the controller: "A *controller* of SSF writes data into the data area of the physical sector Y" (column 2, lines 48-49, emphasis added). That the controller makes this conversion

is also clear from other portions of Niijima, for example at column 3, lines 40-42: "the controller maintains an area in a random access memory for an address translation table".

This distinction can also be illustrated with reference to the figures in Niijima. The potion of Niijima at column 2 cited in the Office Action refers to Figures 1 and 2. As shown in these figures, the logical to physical translation has already been performed in the Address translation table before the address is sent to the SSF. Similarly, with reference to Niijima's Figure 4, which relates to the non-prior art teachings of Niijima, the logical address would converted by the Controller 30 using the Address translation unit 35 in RAM 32, and then it is the *already converted* physical address which is sent to the Flash memory 34. Consequently, there is no "converting on the memory the logical sector address into a corresponding physical sector address" in Niijima.

Consequently, it is respectfully submitted that a rejection of claim 38 under 35 U.S.C. 102(b) as anticipated by Niijima is not well founded and that, for these reasons, claim 38 is also believed allowable. Reconsideration of claim 38 is respectfully requested and an early indication of its allowability is earnestly solicited.

Respectfully submitted,

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